Listing of the Claims:

1. (Previously presented) A thin film transistor array panel for an X-ray

detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and comprising a gate line and a

gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and comprising:

a data line which intersects the gate line;

a source electrode connected to the data line and disposed on the

semiconductor layer; and

a drain electrode disposed on the semiconductor layer separate from

the source electrode;

a photo diode comprising:

a first electrode connected to the drain electrode;

a second electrode which faces the first electrode; and

a photo-conductive layer disposed between the first electrode and the

second electrode;

a passivation layer disposed on the photodiode, the semiconductor layer, the

data wire and the drain electrode, the passivation layer having a contact hole which

exposes the second electrode;

P2002-0078745 OPP051182US PNK-0217 (formerly YOM-0217) Page 2 of 11

Response to Final Office Action filed: September 5, 2008

Reply to Final Office Action of July 7, 2008

a bias signal line disposed on the passivation layer and connected to the

second electrode through the contact hole; and

a light blocking layer disposed directly on the passivation layer and the bias

signal line to cover the photo diode.

2. (Previously presented) The thin film transistor array panel of claim 1,

wherein the photo-conductive layer comprises a first amorphous silicon film

comprising an N type impurity, a second amorphous silicon film disposed on the first

amorphous silicon film and comprising intrinsic amorphous silicon, and a third

amorphous silicon film disposed on the second amorphous silicon film and

comprising a P type impurity.

3. (Previously presented) A thin film transistor array panel for an X-ray

detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and comprising a gate line and a

gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and comprising:

a data line which intersects the gate line;

a source electrode connected to the data line and disposed on the

semiconductor layer; and

P2002-0078745 OPP051182US Page 3 of 11

Response to Final Office Action filed: September 5, 2008

Reply to Final Office Action of July 7, 2008

a drain electrode disposed on the semiconductor layer separate from

the source electrode;

a photo diode comprising:

a first electrode connected to the drain electrode;

a second electrode which faces the first electrode; and

a photo-conductive layer disposed between the first electrode and the

second electrode;

a passivation layer disposed on the photodiode, the semiconductor layer, the

data wire and the drain electrode, the passivation layer having a contact hole which

exposes the second electrode; and

a bias signal line disposed directly on the passivation layer, connected to the

second electrode through the contact hole and comprising a light blocking layer

which covers the photo diode.

4. (Previously presented) The thin film transistor array panel of claim 3,

wherein the photo-conductive layer comprises a first amorphous silicon film

comprising an N type impurity, a second amorphous silicon film disposed on the first

amorphous silicon film and comprising intrinsic amorphous silicon, and a third

amorphous silicon film disposed on the second amorphous silicon film and

comprising a P type impurity.

P2002-0078745 OPP051182US PNK-0217 (formerly YOM-0217) Page 4 of 11

Response to Final Office Action filed: September 5, 2008

Reply to Final Office Action of July 7, 2008

5. (Previously presented) A thin film transistor array panel for an X-ray

detector, the thin film transistor array panel comprising:

a gate wire formed on an insulating substrate and comprising a gate line and a

gate electrode connected to the gate line;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the gate insulating layer and comprising:

a data line which intersects the gate line;

a source electrode connected to the data line and disposed on the

semiconductor layer; and

a drain electrode disposed on the semiconductor layer separate from

the source electrode;

a photo diode comprising:

a first electrode connected to the drain electrode;

a second electrode which faces the first electrode; and

a photo-conductive layer disposed between the first electrode and the

second electrode; and

a bias signal line connected to the second electrode, wherein

the semiconductor layer is disconnected in a region disposed between the

source electrode and the drain electrode, and

the region disposed between the source electrode and the drain electrode is

absent semiconductor material to transmit a signal to the data line.

P2002-0078745 OPP051182US PNK-0217 (formerly YOM-0217) Page 5 of 11

Response to Final Office Action filed: September 5, 2008

Reply to Final Office Action of July 7, 2008

6. (Previously presented) The thin film transistor array panel of claim 5,

wherein the photo-conductive layer comprises a first amorphous silicon film

comprising an N type impurity, a second amorphous silicon film disposed on the first

amorphous silicon film and comprising intrinsic amorphous silicon, and a third

amorphous silicon film disposed on the second amorphous silicon film and

comprising a P type impurity.

P2002-0078745 OPP051182US PNK-0217 (formerly YOM-0217)